Amendments to the Specification:

In the title:

Please replace the title with the following rewritten title:

METHOD AND APPARATUS FOR CANCELLING INTER-SYMBOL INTERFERENCE (ISI) WITHIN A COMMUNICATION CHANNEL

Please amend the paragraph beginning at page 4, line 4 as follows:

Figure 1 illustrates a first embodiment of a FIR filter 10 in accordance with the present invention. The required delay for FIR filter 10 is created by passing the signal directly through a transmission (delay) line 12 on chip. The significant advantage of the passive delay line 12 is its zero power consumption, while other active forms of delay elements especially at multi-GHz range consume significant power. However, generating reasonable delay times (tens of psec and above) using just plane metal lines requires extremely long lengths, making on-chip ~~14n~~ implementation impractical. Therefore, lumped LC transmission lines 14a-14n are utilized to achieve the range of delays expected for the FIR filter.

Please amend the paragraph beginning at page 4, line 12 as follows:

The multiplication stage is performed by passing the output signal from each delay stage through an attenuator that can continuously attenuate the signal from no attenuation ($\alpha i=1$) to complete blocking ($\alpha i=0$). The attenuated signal is then applied to a GM stage/transistor stage 16a-16n that converts the signal voltage into current. Therefore, the output currents of the Gm stages are direct representatives of the delayed version of the signals multiplied by the corresponding filter tap weight (αi). The adder circuit is implemented by ~~the~~ a current summing element ~~18a-18n~~, which is capable of very high-speed analog summing. In this scheme, the output terminals of the Gm stages 16a-16n are connected together to form the signal current addition, and tied to a resistance to implement the current to voltage conversion.

Please amend the paragraph beginning at page 5, line 10 as follows:

Figure 2 illustrates a second embodiment of a FIR filter 30 in accordance with the present invention. In this design, the effective number of delay stages are broken into two branches 32a and 32b where each branch has half the total delay, and thus signal attenuation in each passive branch before amplification by an active stage is half. As Figure 2 clearly demonstrates, in this alternative embodiment, the signal moves in two opposite directions, gets half of the required delay through the bottom branch, is multiplied by the tap coefficient, and added to the top branch where it gets the second half of the delay. One advantage of this approach compared to the Figure 1 FIR filter 10 is the higher power dissipation as the top branch has to have two sides terminated and therefore twice as much power for the same termination resistor 36 value is dissipated. However, by careful design, one can use larger (double) termination resistor for the top branch and adjust the LC delay stages accordingly to re-gain the extra power loss due to two terminations.

Please amend the paragraph beginning at page 6, line 11 as follows:

The tuning circuit 50 comprises an input clock buffer 52, a four stage delay element 54, a differential phase detector 56, and a loop filter 58. A precise system clock is provided to the IC an propagates through four identical inductor/varactor stages. The differential phase detector 56 ~~54~~ senses the rising edge of the clock, the rising edge delayed by 180 degrees, and the rising edge delayed by 360 degrees (a complete period). Any delay difference is translated into a current and fed to the loop filter 58. The loop filter 58 converts the current difference into a voltage value. This voltage output is used to tune the delay of the varactor 60a-60d in such a way that all the sensed clock edges (rising edge, 180 delayed, and 360 delayed) line up. This is a second order feedback loop which tunes the delay of the four inductor/varactor stages in such a way that the delay is exactly one clock cycle. Now if exactly identical inductor/varactor stages are physically laid out (nearby within the same wafer) with the same value of the control voltage (on the varactor), their delay characteristic will mimic the delay of the stages within the tuning stage. This is known as slaving the delay of a separate stage by using a feedback tuning circuit. Therefore, by establishing a voltage on the varactor within a tuning feedback circuit, one can construct precise delay elements through constructing identical stages nearby, and use the same control voltage to only tune the varactor.

Please amend the paragraph beginning at page 9, line 5 as follows:

3. The other method used successfully to combat inter-symbol interference (ISI) so far in multi-Gbps links is transmitter pre-emphasis ~~(2)~~. However, one drawback of the transmit pre-emphasis is that it consumes part of the transmitter power for pre-shaping the output signal. If channel bandwidth is considerably lower than the data rate, the pre-emphasis may require a large portion of the output driver power budget. While in a receiver equalizer the extra filter taps lead to a small power overhead. In

addition, a transmit pre-emphasis approach imposes issues such as interoperability in systems that include far side transmitters ~~on far side does~~ that do not use pre-emphasis, or a medium (e.g., fiber) is not a linear channel.

Please amend the paragraph beginning at page 11, line 12 as follows:

The second issue with the feedback only equalizer is the limited speed of the decision feedback loop that turns into a serious bottleneck for implementation in relatively slow processes like CMOS at multi-GHz speeds. To be able to fully utilize a decision feedback equalizer (DFE) filter, all the previously detected bits must have been resolved ~~resolve~~ at the time of the detection for a current bit. However, due to the limited speed of the comparator, a certain number of bits right after the current bit may not be ready for the use of the feedback filter. Therefore, the feedback equalization (FBE) ~~(FEB)~~ is delayed for as many bit periods that it takes for a sampled data symbol to be resolved. Using this technique allows the decision feedback equalizer (DFE) filter to perform more effective feedback equalizer (FBE) filtering for part of the inter-symbol interference (ISI) that is a certain number of bit periods away from the main data symbol, and leave the equalization of the inter-symbol interference (ISI) close to the symbol to the feed-forward (FFE) filter. Thus, this technique is a suitable approach for channels with relatively large multi-path delays where signal amplitude is fairly large for several bit periods, such as in long multi-mode fibers.